The advent of CMOS technology has revolutionized the field of electronics and has brought forth the invention of various electronic devices with immense computing power and high performance in all domains. Traditionally, higher speed and performance have been the focus of design rather than power consumption. The success of portable laptops and cellular phones has driven the need for low power computing and communication. With the available energy being a fixed value for battery operated devices, the rate of power consumption determines the time between recharges, the lifetime of the battery, and in turn, the features and functionality supported by the device. This tends to put an upper bound on the power dissipation of a device for different operational modes, so as not to affect the functionality.

To help achieve the power goals while being in accordance with Moore's law, innovations in architecture and design strategies are needed to help curb the increasing power dissipation in circuits. Advanced integration of power reduction techniques with CAD tools and the design flow are necessary to make design of low power circuits as easy as possible with the least manual intervention.

The low power techniques used comprehensively today have been integrated with CAD tools, but portability and uniformity details are absent. This thesis details the power reduction techniques that are in use and a new IEEE standard - Unified Power Format (UPF) along with its usage to achieve low power consumption. The application of UPF and Synopsys tools is
illustrated with the designs of an 8 bit ripple carry adder and a 32 bit pipelined CPU designed for low power consumption.

Results show that dynamic power reduces drastically for larger designs with application of UPF. Leakage power reduction is higher with increased technology scaling. From both designs, it is seen that a combination of nominal and high $V_t$ cells gives the best combination of timing and power. It is up to the user to choose and decide the strategies to implement to reduce power.